REMARKS

Claims 1-2, 5, 7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Partovi et al. U.S. Patent 5,353,424.

Claims 13-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Partovi et al. in view of "Fail-Soft Circuit Design in a Cache Memory Control LSI" by Ooi et al.

Claims 1 and 13 are amended. No claims are cancelled or added.

Reconsideration of this application is respectfully requested.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: Improper spelling is used on page 11, lines 1-2 with "serier-coupled". Furthermore, in the description of figure 3, reference is given to steps "310-325", wherein, not all numbers in this range are reflected in the figure. Appropriate correction is required.

In response, Applicants have amended the specification to correct the informalities indicated by the Examiner. In view of Applicants' amendment to the specification, Applicants respectfully request that the Examiner reconsider and withdraw the objections to the specification.

Claim Rejections - 35 USC § 102

Claims 1-2, 5, 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Partovi et al. U.S. Patent 5,353,424 ("Partovi"). Applicants respectfully disagree with the Examiner's assertions and characterizations of the cited reference.

Claim 1, as amended, recites:

> A processor comprising:
> a cache having a plurality of hit lines; and
> a selector to provide a data during a clock cycle from a plurality of memory locations associated with the plurality of hit lines in the cache;
> a multi-hit detection circuit coupled to the hit lines to detect multiple hits in the cache during the clock cycle based on hit signals on the hit lines, the multi-hit detection circuit comprising a NAND gate with transistor pairs; and
> an error flag generated by an inverter output in the multi-hit detection circuit during the clock cycle to indicate that the data provided during the clock cycle is invalid if multiple cache hits are detected, the error flag to indicate that the data provided during the clock cycle is valid if a single cache hit is detected.

Partovi is generally directed to providing a fast tag comparator and bank select in a set-associative cache. In contrast with Claim 1, Partovi does not teach or suggest an error flag generated during a clock cycle to indicate that the data provided during the clock cycle is invalid if multiple cache hits are detected, much less that such error flag is to indicate that the data is valid if a singe cache hit is detected. Partovi described he data memory of a cache as including two banks that provide four possible outcomes for a compare operation: both banks miss, left bank hits, right bank hits, and both banks hit. (*See* Abstract.) However, as taught by Partovi, neither bank is selected when both left and right tags indicate a hit, which Partovi indicates is a condition where the same tag is stored in both the left and right banks which is an anomalous situation indicating an error. (Col. 12, lines 15-20.)

Partovi does disclose that a miss condition should be signaled when a hit is detected for both the right bank and left bank, (col. 12, lines 21-23), however, that is something completely different from a multi-hit detection circuit generating an error flag to indicate that data provided during the clock cycle is invalid of multiple cache hits are detected, as in Claim 1. Apposite to Claim 1, we submit that the issuance of a miss condition, as taught by Partovi, does not teach or suggest an error flag generated to indicate that data provided during a clock cycle is invalid if multiple cache hits are detected, as in Claim 1.

Furthermore, the same error flag will indicate that the data provided during the clock cycle is valid if a single cache hit is detected, as in Claim 1. We submit that Partovi fails to disclose the generation of an error signal to indicate that data provided during a clock cycle is valid if a single cache hit is detected, as in Claim 1.

According to the Examiner, the above-recited features of Claim 1 are disclosed by Partovi at column 2, lines 59-63; column 4, lines 20-23; column 6, lines 19-42; column 11, lines 23-24; and column 15, lines 15-22 (*see* pages 2 and 3, paragraph 4 of the Office Action mailed 2/8/07.) However, the Examiner's characterization of Partovi, as well as the passages cited by Partovi, are directed to prohibiting the selection of a bank when a multiple bank hit is detected and issuance or signaling of a miss condition in such situations (*see* col. 12, lines 15-26.) Neither these sections nor any other disclosure in Partovi teaches or suggests the generation of an error signal to indicate that the data provided during the clock cycle is invalid if a multiple cache hit is detected, much less that the same error flag is used to indicate that the data is valid if a single cache hit is detected, as in Claim 1.

For each of the above reasons, therefore, Claim 1 and all claims which depend on it are patentable over the cited art. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 1, 2, 5 and 7.

Each of Applicants' other independent claims includes limitations similar to those in Claim 1 discussed above. Furthermore, none of the references of record rectify the deficiencies of Partovi in teaching or suggesting an error flag which is used to indicate the invalidity of data when a multiple cache hit is detected, as well as the validity of such data when a single cache hit is detected, as in Claim 21.

Therefore, all of Applicants' other independent claims, and all claims which depend on them, are patentable over the cited art, for similar reasons. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 13-16.

Dependent Claims

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicant's silence regarding any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

Allowable Subject Matter

Claims 6 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim. Applicants respectfully thank the Examiner for recognizing the allowability of Claims 6 and 17. However, for at least the reasons

provided above, Applicants respectfully submit that Claims 6 and 17, based on their dependencies from Claims 1 and 13, respectively, are also patentable over the cited art, as well as the references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the objection to Claims 6 and 17, and allow such claims, based on their dependencies from Claims 1 and 13.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: 5/7/07 By: _____
Joseph Lutz, Reg. No. 43,765

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
Telephone (310) 207-3800
Facsimile (310) 820-5988

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

Suzanne Johnston 5/7/07
Date